REMARKS

Claims 1-47 are pending in this application.

Claims 1-26, 28-31, 33-34, 36-43, 45-47 are rejected under 35 U.S.C. § 102(b).

Claims 27, 32, 35 and 44 are objected to.

Claims 1-47 remain in the case for reconsideration.

No new subject matter has been added.

Applicant respectfully request reconsideration and allowance of the claims in light of above amendments and following remarks.

Claim Objections

Claims 27, 32, 35 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims have been rewritten in independent form and therefore are in condition for allowance.

Claim Rejections

Claims 1-26, 28-31, 33-34, 36-43, 45-47 are rejected under 35 U.S.C. § 102(b) as being anticipated by Merchant et al. (US Patent No. 6,584,106 B1). Claims 7, 19 and 29 are rejected under 35 USC 103(a) as being unpatentable over Merchant et al. in view of Opalka et al.

Claim 1 has been amended to specify a first ingress interface for receiving from a source port packets having associated ingress flows and assigning ingress flow values to the packets associated with the ingress flows that identify packets having similar Quality of Service processing requirements and storing the packets in an ingress memory; a second ingress interface for outputting packets or cells to a switch fabric; and an ingress controller that queues the packets or cells in the ingress memory for sending to an egress memory via the switch fabric according to the associated ingress flow values.

This is clearly shown in FIGS. 1-10. For example, FIG. 1A shows per flow queuing 21 to a switch fabric 22 and FIG. 5A shows packets A, B and C being assigned and being queued for sending over the switch fabric to the output queues according to ingress flow ID values.

The Examiner states that Merchant teaches a memory hub that includes a first ingress interface for receiving from a source port packets having associated ingress flows (FIG. 3A, column 6, lines 9-15). However, nowhere does Merchant teach assigning internal ingress flows values to the packets that identify packets having similar Quality of Service processing requirements.

The examiner also states that Merchant in FIG. 3A, column 6, lines 32-35, lines 40-42 suggests an ingress controller that queues the packets according to the associated ingress flows.

Nothing in Merchant discusses an ingress interface sending packets from an ingress memory through a switch fabric to an egress memory. Merchant just shows queuing logic 74 that sends packets to an external memory 36. For example, column 6, lines 32-35 state that queuing logic 74 transfers received data from the corresponding internal receiver FIFO to the external memory 36. Merchant does not have a switching fabric that is used to transfer packets from an ingress memory to an egress memory as specified in claim 1.

Regardless, Merchant does not include an ingress controller that queues packets or cells in the ingress memory for sending over a switch fabric according to the Quality of Service processing requirements identified by the ingress flow values.

As stated in the specification at page 5, line 25: "The architecture 34 combines traffic management with backplane interfacing for processing packets on a per flow basis. This eliminates one complex packet queuing stage from the overall network processing device as well as eliminating one set of interfaces."

Merchant does not combine packet traffic management with backplane switch fabric interfacing at all and particularly as specified in claim 1 where the packets are transferred over a switch fabric according to the ingress flow ID values.

Claim 2 is amended stating the traffic manager modifies an assigned Class of Service for the packets and assigns the modified Class of Service to the packets before being output to the switch fabric. This limitation is similar to the limitation in claim 27 that has already been indicated by the Examiner as allowable.

Claim 5 recites a memory hub that includes, among other features, "an ingress traffic manager that schedules how the packets or cells are output to the switch, wherein the ingress controller and the ingress traffic manager are *separate circuits operating on separate integrated circuits.*" The Examiner asserts that Merchant teaches that "the ingress controller and the ingress traffic manager are separate circuits operating on separate integrated circuits

(FIG. 3A, FIG. 3B) referenced by Queuing Logic as separate unit from internal Rule Checker 40." This assertion is incorrect, however. Indeed, FIG. 3 in Merchant, only "depicts the switch subsystem 42 of FIG. 2," which is a block diagram of the multiport switch 12. col. 6, line 4 and col. 4, line 10. Thus, referring to FIGS. 2 and 3, it is clear that the alleged Queuing Logic and Rule Checker units are *on the same circuit, namely on switch board 12.*

Therefore, Merchant fails to teach or disclose an ingress traffic manager that schedules how the packets or cells are output to the switch, wherein the ingress controller and the ingress traffic manager are *separate circuits operating on separate integrated circuits.* Consequently, Merchant fails to anticipate amended claim 1 because Merchant does not expressly or inherently teach each and every element as set forth in amended claim 1 (MPEP 2131 "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.")

Claims 12 and 39 also specify the memory hub as an integrated circuit having a first interface for communicating with one or more source ports, a second interface for communicating with an ingress traffic manager, a third interface for communicating with a switch fabric and a fourth interface for communicating with an external memory. This is clearly shown in FIG. 1A. Neither Merchant or any of the other cited art suggest this configuration.

Claim 8 has been amended to specify the ingress flow values as being assigned independently of the source port receiving the packets. Claims 20 and 22 describe the ingress flow values being assigned independently of a source or destination address. This is shown in FIG. 5 where the packets A, B and C from the same source port are assigned different ingress flow ID values according to different Quality of Service egress flows.

There is nothing in Merchant that suggests this limitation. The examiner states that Merchant at column 5, lines 30-38 teaches in ingress traffic manager that schedules outputting of packets on a per flow basis or Class of Service bases. But nowhere in Merchant, including column 5, lines 30-38, are ingress flow values independently of the source port, or source address, or destination address associated with the packet used for sending the packets across a switch fabric. Column 5, lines 30-38 of Merchant describes a forwarding descriptor that includes a priority class. However, there is no suggestion that this priority class is used as a basis for transferring packets over a switch fabric to an egress memory.

Claim 13 has been amended to specify the egress controller tracking packet size information for the egress flows and queuing the packets for outputting to destination ports according to the tracked packet size information. This is similar to the limitations in claim 35 which is indicated as allowable by the Examiner.

Claim 17 has been amended to specify the first ingress interface storing the packets in an external ingress memory and the second ingress interface outputting the packets from the external ingress memory through the switch fabric to an external egress memory according to the ingress flow values associated with the packets.

Conversely, Merchant does not include an external ingress memory for initially storing the ingress packets and an external egress memory for receiving the packets over the switch fabric from the external ingress memory.

Claim 20 has limitations similar to claim 1 and is therefore patentable for the same reasons

Claim 38 recites a memory hub that includes, among other features, "*a controller* that *queues* the packets or packet fragments in a memory according to the associated flow Ids and *dequeues* the packets from the memory according to the associated flow Ids." It is alleged that Merchant teaches "a controller that queues the packet or packet fragment in a memory according to the associated flow Ids (column 5 lines 30-36) referenced by OutPut Queue Write Side Mgmt Side Mgmt Port 68a which uses frame pointers associated to ports to fetch data from memory for management processing." This assertion is incorrect, however.

In contrast, Merchant only teaches that "the port vector is examined by the port vector FIFO 56 to determine which particular output queue should receive the associated frame pointer. The port vector FIFO 56 places the frame pointer into the top of the appropriate queue 58 and/or 68." col. 8, lines 23-28. Thus, reference 68a in FIG. 3A is clearly an output queue port not *a controller for queuing and dequeuing the packets* in a memory according to associated flow Ids.

Thus, Merchant fails to teach or disclose *a controller* that *queues* the packets or packet fragments in a memory according to the associated flow Ids and *dequeues* the packets from the memory according to the associated flow Ids. Consequently, Merchant fails to anticipate amended claim 38 because Merchant does not expressly or inherently teach each and every element as set forth in amended claim 38 (MPEP 2131 "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.")

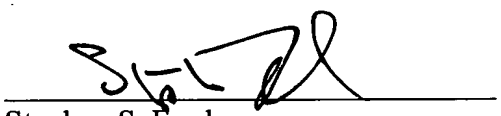
Claims 39-46 are directly or indirectly dependent on amended claim 38, and for at least the reasons given for claim 1, these claims are believed to be allowable over Merchant. The Examiner has already indicated allowability of claim 44.

Claim 47 has been amended to include limitations similar to allowed claim 35 and is therefore allowable for the same reason as claim 35.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-47 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,



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Annotated Sheet Showing Changes

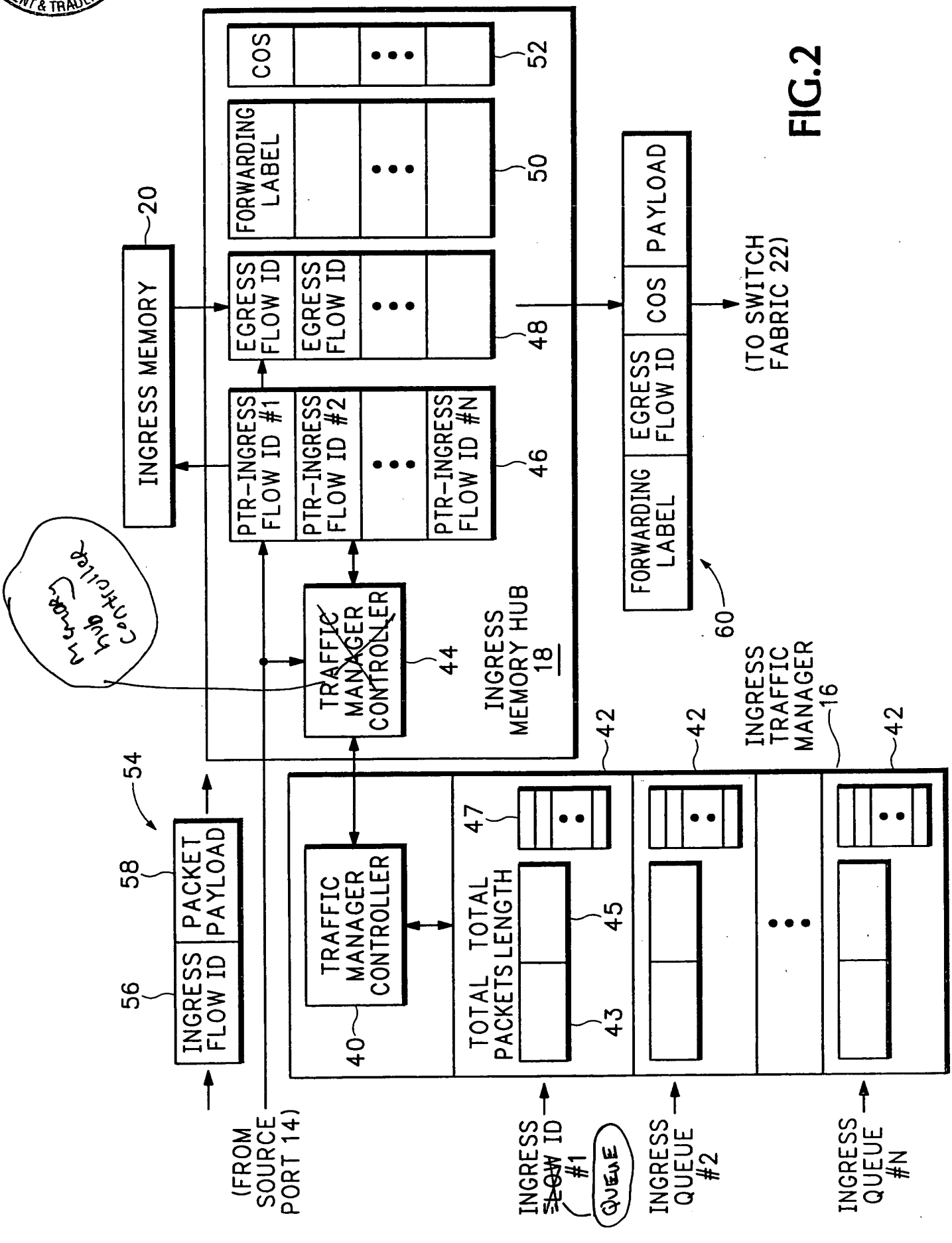

FIG.2

Annotated Sheet Showing Changes

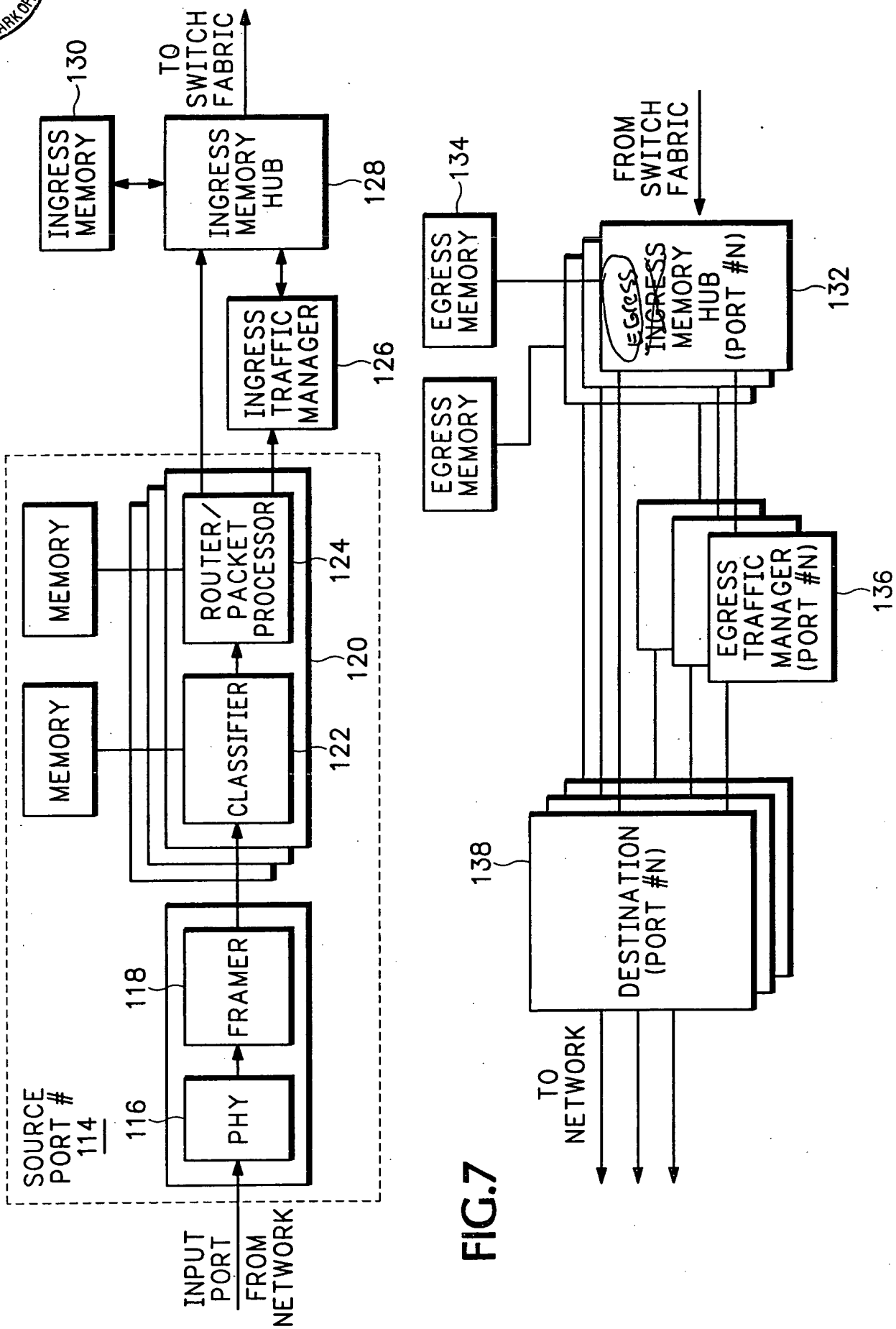

FIG.7

IN THE DRAWINGS

As requested by the Examiner, attached are corrected drawings showing changes made, as well as replacements sheets.